USER MANUAL

UM9701

Version 3.0

REVISION HISTORY

Version	Remarks
0.1	DRAFT; 14.08.96
0.2	Update I²C REGs 24,25; 20.08.96
0.3	Update REG7: ENA_HWE_ROUGH; 21.08.96
1.0	First Release; refers to BESIC-SW from V0.34 until V1.0; 31.10.96 (This UM describes the I²C interface of the BESIC for a single memory concept or a PROZONIC concept. The µC ROM of the first BESIC samples contain this interface. MELZONIC control (SAA4991) is not possible via the I²C interface described in this document)
2.0	Second Release; refers to BESIC-SW starting with V2.0; 28.02.97 This document describes a new I²C interface of the BESIC including the MELZONIC control in addition to the features described in the first release document. An external µC ROM of the first BESIC samples will contain this new I²C interface. A new BESIC version, which will be developed, contains the new interface.
3.0	Release Version 3.0, 12.06.97; refers to BESIC-SW starting with V5.0; 05.05.97

USER MANUAL

UM9701
I²C-bus Register Specification for BESIC

Report No.: UM9701

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Preface

The specification describes the I²C-bus register interface of an IPQ slave microcontroller (80C51 core), which is integrated in the BESIC (SAA 4974/SAA 4977).

The BESIC is a videoprocessing IC providing analog interfacing, video enhancing features, memory controlling and the embedded 80C51 microprocessor core. The slave IPQ µC is used as an interpreter between a main (master) µC and the Datapath Control in BESIC as well as the direct ECO control (internal) and, in case of a two field memory concept, also the PROZONIC (SAA4990; external) or MELZONIC (SAA4991;external).

CONTENTS

1. Introduction

1.1 Definitions, Acronyms and Abbreviations

BESIC	Single Chip concept for IPQ with integrated memory controller, µC, AD/DA part, PLLs 2 concepts available: 1. SAA 4974 (LOBESIC; production SW; without analog control part; applicable with MELZONIC SAA 4991 together with two field memories SAA 4955 or only one single field memory SAA 4956 (contains noise reduction feature) for simple 100 Hz AABB mode) 2. SAA 4977 (basic test SW; applicable with SAA 4991 or SAA 4990 together with two field memories or simple 100 Hz with one field memory only) Third concept planned with analog control part, production SW status; applicable as low-end 100 Hz concept with one SAA 4956 or mid/high-end concepts with the SAA 4990 or SAA 4991 together with two field memories SAA 4955
ECO	Economy Controller (integrated in BESIC)
HEX	Hexadecimal program file
HOST interface	BESIC Interface towards 8051 microprocessor core
IPQCS	Improved Picture Quality Control Software
IPQ µC	Improved Picture Quality slave microcontroller
LFR	Line Flicker Reduction by median filtering
MELZONIC	Motion Estimation and compensation, Line flicker reduction, ZOom and Noise reduction IC (SAA 4991)
MPIP	Multi picture in picture with external PIP processor
NR	Noise reduction (adaptive)
PROZONIC	Progressive Scan, Zoom and Noise Reduction IC (SAA 4990)
VDFL	Vertical deflection pulse generated by the memory controller in BESIC

1.2 References

[SCP] Philips Semiconductors Software Creation Process V1.0; Wilko van Asseldonk, Marc de Smet; April 9th, 1996

[TDS] Tentative Device Specification for BESIC; 06.08.96; A. Kannengiesser

[TDS-CP] Tentative Device Specification Control Part BESIC V1.2; 13.02.97; G. Stäcker, H. Waterholter

[UCMS-OF] 80C51 microcontroller order form

[UCMS-CS] 80C51 microcontroller Core Specification V1.2; 22.02.96; P. Klapproth

[DPCR] Datapath Control Register; 13.08.96; A. Kannengiesser

2. General

The IPQ µC reads register bytes via the I²C-bus from the master µC and sends itself 1 status byte plus following read registers whenever addressed with R/W = 1. The I²C register bytes received are written into the µCs RAM.

The new microcontroller software for BESIC (Version numbers V5.0 or higher) contains all functionality for the MELZONIC concept and the single field concept. Additionally the PROZONIC concept is planned to be supported by an upgraded software version for BESIC.

TABLE 1 Functions supported by the concepts

Function	Single field concept	Melzonic concept	Prozonic concept
AABB mode	x	x	x
Line flicker reduction		x	x
Motion compensation		x	
Noise and cross colour reduction	x (with the SAA 4956)	x	x
Progressive Scan		x	x
Reduction of FM drop-outs		x	x
Vertical Zoom		x	x
Support of MPIP		x	x
Still picture	x (field based)	x (frame based)	x (frame based)
Generator mode	x	x	x
Digital CTI	x	x	x
Luminance peaking and coring			
Variable luminance delay	x	x	x
Sidepanel generation	x	x	x
Screen fade	x	x	x
option for downgrade to one-clock system	x	x	x

3. I²C-bus interface

3.1 Definition of the interface

The interface of the IPQ µC is realized with a hardware I²C-bus.

The slave address of the IPQ µC is 68h:

Slave address = 0 1 1 0 1 0 0 R/W.

The IPQ µC can either act as a slave receiver or a slave transmitter. In the slave receiver mode the IPQ µC reads I²C register data bytes from the main controller which then acts as a master transmitter. In the slave transmitter mode the IPQ µC sends status information to the main µC which works as a master receiver reading the byte information.

3.2 Sending data to the IPQ µC

3.2.1 I²C transmission protocol

The transmission protocol has the following format:

Start	Slave address 68h	Ack	Subad-dress	Ack	REG1	Ack	.....	Ack	REGx	Ack	Stop

After having addressed the IPQ µC with its slave address the master µC transmits the subaddress plus following register bytes over the I²C-bus. The number of register bytes which are transmitted after the transmission of the subaddress must not exceed 60 bytes. It is possible to transmit just one single register byte after having sent the slaveaddress plus subaddress (3 bytes package).

The IPQ µC acknowledges always all register bytes independent of their contents. If the master µC transmits more than the maximum number of register bytes, the slave µC will acknowledge the following bytes, but will not store them in the internal RAM.

Subaddresses starting from 30h onwards indicate, that datapath control registers are to be serviced.

3.2.2 I²C function register data format

[Default hex values in brackets]

Table 2: I²C-Register REG1: Subaddress 00 hex [00]

Bit	Name	Function
0		reserved
1		reserved
2	G_MODE	0: normal mode 1: generator mode on
3		to be cleared
4	AFF	acquisition field frequency (50/60 Hz): 0 = 50 Hz, 1 = 60 Hz
5		reserved
6		reserved
7	INIT	initialize BESIC, MELZONIC or PROZONIC: 0 = off, 1 = on

Table 3: I²C-Register REG2 (FIELD CONTROL); Subaddress 01 hex [01]

Bit	Name	Function
0	LFR	line flicker reduction mode: 0 = off (AABB mode), 1 = on (AA*B*B, ABAB raster)
1	NR_AABB	0: normal mode 1: noise reduced AABB mode (LFR bit has to be set to 0) (PROZONIC concept with one single memory)
2	AABB_CORR	0: normal mode 1: VRE1 shift 50 Hz wise in case LFR=0 (Special test mode)
3	CORR_PHASE	0: increment VRE1 (in case AABB_CORR=1) 1: decrement VRE1 (in case AABB_CORR=1)
4	MOVIE	Forced Movie mode (ABAB raster) 0: off 1: on
5	PHASE	Forced Phase Flag to be set in combination with MOVIE 0: normal mode 1: 180 deg. phase shift (BCBC)
6	AUTO_MOVIE	0: normal mode 1: automatic movie mode activated. In case of a detected movie source, the field processing will switch to movie mode and the correct movie phase will be processed (MOVIE_FLAG, PHASE_FLAG are readable via STATUS register)
7	STP	still picture mode 0: off 1: on (one field out of AABB, full frame median filtered out of LFR)

Table 4: I²C-Register REG3 (VZOOM): Subaddress 02 hex [10]

Bit	Name	Function				
0	VZOOM_0	Vertival zoom bit 0				
1	VZOOM_1	Vertical zoom bit 1				
2	VZOOM_2	Vertical zoom bit 2				
3	VZOOM_3	Vertical zoom bit 3				
		V3	V2	V1	V0	Conversion factor NATURAL MOTION (in brackets values for NATURAL_MOTION=0, LFR=1) xx: invalid mode (Auto vshift:BUF_REG8 values)
		0	0	0	0	xx (1.06; auto vshift: 8A hex)
		0	0	0	1	reserved
		0	0	1	0	1.1 (1.1; auto vshift: 8E hex)
		0	0	1	1	reserved
		0	1	0	0	xx (1.15; auto vshift: 94 hex)
		0	1	0	1	reserved
		0	1	1	0	xx (1.2; auto vshift: 99 hex)
		0	1	1	1	reserved
		1	0	0	0	1.25 (1.25; auto vshift: 9F hex)
		1	0	0	1	reserved
		1	0	1	0	xx (1.3; auto vshift: A3 hex)
		1	0	1	1	reserved
		1	1	0	0	1.33 (1.33; auto vshift: A6 hex)
		1	1	0	1	reserved
		1	1	1	0	1.5 (1.5)
		1	1	1	1	reserved
4	NATURAL_MOTION	0: Natural Motion off 1: Natural Motion active				
5	ENA_LFR_PHASE	0: fixed mode 1: phase adaption for movie source in LFR mode, only for PRO-ZONIC				
6	SAT_MODE	Satellite Mode (removes FM drop-outs) 0: off (Natural Motion, LFR, AABB, AUTO_MOVIE or MOVIE mode active) 1: on (Natural Motion, LFR, AABB, AUTO_MOVIE and MOVIE not active)				
7	VZOOM	0: Vertical Zoom mode not active 1: Vertical Zoom mode active				

Table 5: I²C-Register REG4 (External Multi PIP): Subaddress 03 hex [00]

Bit	Name	Function
0	POS0	PIP position bit 0
1	POS1	PIP position bit 1
2	POS2	PIP position bit 2
3	POS3	PIP position bit 3
4		reserved
5	NPIP	number of PIP's: 0 = 3x3 PIP's, 1 = 4x3 PIP's (4x3 not implemented)
6	MPIP	External Multi-PIP: 0 = off, 1 = on
7	SPIP	NTSC PIP: 0 = 50 Hz PIP, 1 = 60 Hz PIP

Table 6: I²C-Register REG5 (NR, SCREEN FADE): Subaddress 04 hex [02]

Bit	Name	Function		
0	NR0	noise reduction bit 0		
1	NR1	noise reduction bit 1		
		NR1	NR0	noise reduction
		0	0	off
		0	1	low
		1	0	middle
		1	1	high
2	SPS0	split screen bit 0		
3	SPS1	split screen bit 1		
		SPS1	SPS0	split screen
		0	X	off
		1	0	horizontal
		1	1	vertical
4	SCF0	screen fade bit 0		
5	SCF1	screen fade bit 1		
		SCF1	SCF0	screen fade
		0	X	OFF
		1	0	fade in
		1	1	fade out
6	NR_INTERR_CTRL	0: default 1: noise reduction processing (bits 1,2) is cancelled each second for the duration of one single display field		
7	PSC	0: default mode 1: Progressive Scan mode		

Table 7: I²C-Register REG6 (ENABLE DIRECT REG. ACCESS): Subaddress 05 hex [00]

Bit	Name	Function
0	SET_HOR_DEL	0: normal mode (HOR_DELAYS=0) 1: HOR_DELAYS value taken from REG12 (direct PROZONIC/ MELZONIC access).
		to be cleared
2	SET_HRE	0: normal mode 1: take HRESTA/STO settings from REGs 15, 16
3	SET_HDDEL	0: normal mode 1: take HDDEL setting from REG17
4	SET_HDMSB	0: normal mode 1: take HDMSB setting from REG18
5	SET_VDMSB	0: normal mode 1: take VDMSB setting from REG19
6	SET_HBDA	0: normal mode 1: set HBDASTA/STO ECO values direct via I²C REGs 20, 21
7	SET_HWE_MAIN_ DELAY	0: normal mode 1: HWE main delay via REG 22

Table 8: I²C-Register REG7: Subaddress 06 hex [00]

Bit	Name	Function
0	SET_HBOX	0: default mode 1: direct control of HBOX_START/STOP via I²C REGs 31, 32
1		to be cleared
2	MANU_VSHIFT	0: VSHIFT for VZOOM is done automatically if NATURAL_MOTION=0 and LFR=1 or FSFM=1 1: VSHIFT for VZOOM (LFR=0 or FSFM=0) via BUF_REG8
3	SET_VBDA	0: default mode 1: direct VBDASTA/STO via REGs 29, 30
4		to be cleared
5	SET_VAMSB	0: default 1: direct VAMSB control via I²C REG24
6	SET_HDAV	0: default 1: direct HDAVSTA/STO control via I²C REGs 25, 26
7		to be cleared

Table 9: I²C-Register REG8 (VWE DELAY): Subaddress 07 hex [00]

Bit	Name	Function
0	VWED0	VWE delay bit 0
1	VWED1	VWE delay bit 1
2	VWED2	VWE delay bit 2
3	VWED3	VWE delay bit 3
4	VWED4	VWE delay bit 4
5	VWED5	VWE delay bit 5
6	VWED6	VWE delay bit 6
7	VWEX	0 = off, normal mode 1 = on, reduced vertical write window shiftable by VWED0...D6

Table 10: I²C-Register REG9 (Test-REG: BLANK FIELDS): Subaddress 08 hex [80]

Bit	Name	Function				
0	BLANK_F0	blank field 0				
1	BLANK_F1	blank field 1				
2	BLANK_F2	blank field 2				
3	BLANK_F3	blank field 3				
4	HWEF0	HWE fine delay offset to default, bit 0				
5	HWEF1	HWE fine delay offset to default, bit 1				
6	HWEF2	HWE fine delay offset to default, bit 2				
7	HWEF3	HWE fine delay offset to default, bit 3				
		7	6	5	4	
		0	0	0	0	HWE default -8(16) steps (1 step = 4 clocks)
		.	.	.	.	....
		0	1	1	1	HWE default -1(2) steps
		1	0	0	0	HWE default setting
		1	0	0	1	HWE default +1(2) steps
		.	.	.	.	....
		1	1	1	1	HWE default +7(14) steps

Table 11: I²C-Register REG10: Subaddress 09 hex [00]

Bit	Name	Function
0	FSFM	Forced single field mode, to be set for changing of zoom factors (automatic VSHIFT control, in case MANU_VSHIFT=0)
1	ENA_NM_CONTROL	0: default 1: bad limit setting taken from I²C REG 42, reliability threshhold taken from I²C REG 43
2	SET_NR	0: default 1: direct noise reduction control via REGs 35...41
3	FILL	0: default 1. fill screen with color selected via REGs 33, 34
4	DIGITAL_COLOR_ DECODER_ CONCEPT	0: Analog color decoder concept 1: Digital color decoder concept (internal acquisition PLL switched off; external clock, 16 MHz line locked expected)
5	CLR_MOVIE	0: default mode 1: clear MOVIE_FLAG (forced)
6		to be cleared
7		to be cleared

Table 12: I²C-Register REG11 (Port Settings): Subaddress 0A hex [30]

Bit	Name	Function
0	P11	0: clear port pin P1.1 1: set port pin P1.1
1	P12	0: clear port pin P1.2 1: set port pin P1.2
2	P14	0: clear port pin P1.4 1: set port pin P1.4
3	P15	0: clear port pin P1.5 1: set port pin P1.5
4	MELZ_PROZ	Software selection, only valid if SW_HW=1 0: PROZONIC 1: MELZONIC
5	SW_HW	enable the software selection between PROZONIC/MELZONIC 0: Hardware selection via Pin P1.3 1: Software selection with MELZ_PROZ
6	SEL_FRM	0:default (SFR bit, VAMSB, is set) 1: SFR bit (VAMSB register memory controller part) is cleared
7		to be cleared

Table 13: I²C Register REG12 (HOR_DELAYS): Subaddress 0B hex [28]

Bit	Name	Function
0 ... 7	HOR_DELAYS	direct PROZONIC/MELZONIC register access

Table 14: I²C Register REG13 (reserved): Subaddress 0C hex [xx]

Bit	Name	Function
0 ... 7		reserved

Table 15: I²C Register REG14 (reserved): Subaddress 0D hex [xx]

Bit	Name	Function
0 ... 7		reserved

Table 16: I²C Register REG15 (HRESTA): Subaddress 0E hex [1F]

Bit	Name	Function
0 ... 7	HRESTA	direct ECO register access

Table 17: I²C Register REG16 (HRESTO): Subaddress 0F hex [C3]

Bit	Name	Function
0 ... 7	HRESTO	direct ECO register access

Table 18: I²C Register REG17 (HDDEL): Subaddress 10 hex [00]

Bit	Name	Function
0 ... 7	HDDEL	direct ECO register access bit 3: fine delay of HBLND needs to be cleared !

Table 19: I²C Register REG18 (HDMSB): Subaddress 11 hex [AA]

Bit	Name	Function
0 ... 7	HDMSB	direct ECO register access bit 7 (MSB): MSB of HBLNDSTO needs to be set bit 6: MSB of HBLNDSTA needs to be cleared

Table 20: I²C Register REG19 (VDMSB): Subaddress 12 hex [0A]

Bit	Name	Function
0 ... 7	VDMSB	direct ECO register access bit 0: MSB of VRESTA needs to be cleared bit 1: MSB of VRESTO needs to be set

Table 21: I²C Register REG20 (HBDASTA): Subaddress 13 hex [52]

Bit	Name	Function
0 ... 7	HBDASTA	direct ECO register access

Table 22: I²C Register REG21 (HBDASTO): Subaddress 14 hex [F2]

Bit	Name	Function
0 ... 7	HBDASTO	direct ECO register access

Table 23: I²C Register REG22 (HWE MAIN DELAY): Subaddress 15 hex [32]

Bit	Name	Function
0 ... 7	HWE_MAIN_DELAY	Coarse shift of HWE

Table 24: I²C Register REG23: Subaddress 16 hex [xx]

Bit	Name	Function
0 ... 7		reserved

Table 25: I²C Register REG24 (VAMSB): Subaddress 17 hex [06]

Bit	Name	Function
0 ... 7	VAMSB	direct ECO register access bit 0: MSB of VWESTA needs to be cleared bit 1: MSB of VWESTO needs to be set

Table 26: I²C Register REG25 (HDAVSTA): Subaddress 18 hex [05]

Bit	Name	Function
0 ... 7	HDAVSTA	direct ECO register access

Table 27: I²C Register REG26 (HDAVSTO): Subaddress 19 hex [A9]

Bit	Name	Function
0 ... 7	HDAVSTO	direct ECO register access

Table 28: I²C Register REG27 (reserved): Subaddress 1A hex [xx]

Bit	Name	Function
0 ... 7		reserved

Table 29: I²C Register REG28 (reserved): Subaddress 1B hex [xx]

Bit	Name	Function
0 ... 7		reserved

Table 30: I²C Register REG29 (VBDASTA): Subaddress 1C hex [15]

Bit	Name	Function
0 ... 7	VBDASTA	direct ECO register access

Table 31: I²C Register REG30 (VBDASTO): Subaddress 1D hex [31]

Bit	Name	Function
0 ... 7	VBDASTO	direct ECO register access

Table 32: I²C Register REG31 (HBOX_START): Subaddress 1E hex [00]

Bit	Name	Function
0 ... 7	HBOX_START	direct PROZONIC/MELZONIC register access

Table 33: I²C Register REG32 (HBOX_STOP): Subaddress 1F hex [00]

Bit	Name	Function
0 ... 7	HBOX_STOP	direct PROZONIC/MELZONIC register access

Table 34: I²C Register REG33 (FIXCOL_Y): Subaddress 20 hex [10]

Bit	Name	Function
0 ... 7	FIXCOL_Y	fixed Y value in case FILL=1

Table 35: I²C Register REG34 (FIXCOL_UV): Subaddress 21 hex [00]

Bit	Name	Function
0 ... 7	FIXCOL_UV	fixed UV value in case FILL=1

Table 36: I²C Register REGs 35...41: Subaddresses 22...28 hex

Subaddress (hex)	Name	Function
22	KSTEP01	direct MELZONIC control
23	KSTEP23	direct MELZONIC control
24	KSTEP45	direct MELZONIC control
25	KSTEP67	direct MELZONIC control
26	KFIXED	direct MELZONIC control
27	TFILTER12	direct MELZONIC control
28	DEF	direct MELZONIC control

Table 37: I²C Register REG42 (BAD_LIMIT): Subaddress 29 hex [40]

Bit	Name	Function
0 ... 7	BAD_LIMIT	direct BAD_LIMIT setting if ENA_NM_CONTROL=1 (Threshold for NR_BAD_RANGES, MELZONIC control)

Table 38: I²C Register REG43 (RELIABILITY_SEL): Subaddress 2A hex [30]

Bit	Name	Function
0 ... 7	RELIABILITY_SEL	direct MELZONIC register access if ENA_NM_CONTROL=1

3.2.3 I²C translater register data format

Next subaddress for the following I²C registers will be 30h !

Acquisition part:

Table 39: I²C Translater Register 0 (ACQ_0): Subaddress 30 hex

Bit	Name	Host address (hex)	Default value (hex)	Function
0 ... 7	AGC_Y	0150	66	AGC gain for Y channel (2´s complement rel 0 dB): upper 8 bits

Table 40: I²C Translater Register 1 (ACQ_1): Subaddress 31 hex

Bit	Name	Host address (hex)	Default value (hex)	Function
0 ... 7	AGC_UV	0151	90	AGC gain for U and V channel (2´s complement rel 0 dB): upper 8 bits

Table 41: I²C Translater Register 2 (ACQ_2): Subaddress 32 hex

Bit	Name	Host address (hex)	Default value (hex)	Function
0	AGC_Y_LSB	0152	00	AGC gain for Y channel LSB
1	AGC_UV_LSB			AGC gain for UV channel LSB
2	standby_f			1: frontend in standby mode
3	aaf_bypass			1: bypass for prefilter
4				reserved
5				reserved
6				reserved
7				reserved

Table 42: I²C Translater Register 3 (ACQ_3): Subaddress 33 hex

Bit	Name	Host address (hex)	Default value (hex)	Function		
0..1	UVclcorrect_mode	0153	00	Bit1	Bit0	UV clamp mode
				0	0	auto
				0	1	fixed
				1	0	keep
				1	1	-
2..4	Uclcorrect_fval		000	fixed value clamp corr. U channel		
5..7	Vclcorrect_fval		000	fixed value clamp corr. V channel		

Table 43: I²C Translater Register 4 (ACQ_4): Subaddress 34 hex

Bit	Name	Host address (hex)	Default value (hex)	Function		
0..1	UVcoring	0154	00	Bit1	Bit0	UV coring level
				0	0	0
				0	1	+/- 0,5
				1	0	+/- 1
				1	1	+/- 2
2..3	mff_width		01	Bit1	Bit0	majority filter setting
				0	0	1
				0	1	3
				1	0	5
				1	1	7
4..5	UVcl_tau		00	Bit1	Bit0	vertical filtering of measured clamp
				0	0	
				0	1	
				1	0	
				1	1	
6	compress		0	0: compression off 1: compression on		
7	comp_mode		0	0: 14:9 compression mode 1: 16:9 compression mode		

Table 44: I²C Translater Register 5 (ACQ_5): Subaddress 35 hex

Bit	Name	Host address (hex)	Default value (hex)	Function			
0..2	ydelay	0155	010	Bit2	Bit1	Bit0	variable Y-delay
				0	0	0	-2
				0	0	1	-1
				0	1	0	0
				0	1	1	1
				1	0	0	2
				1	0	1	-
				1	1	0	-
				1	1	1	-
3..4	overl_comp		01	Bit1	Bit0	overload threshold	
				0	0	216	
				0	1	224	
				1	0	232	
				1	1	240	
5	fill_mem			0: default 1: fill memory with constant value			
6				reserved			
7				reserved			

Display part:

Table 45: I²C Translater Register 6 (DCTI_0): Subaddress 36 hex

Bit	Name	Host address (hex)	Default value (hex)	Function			
0..2	dcti_gain	01D1	010	Bit2	Bit1	Bit0	dcti gain
				0	0	0	0
				0	0	1	1
				0	1	0	2
				0	1	1	3
				1	0	0	4
				1	0	1	5
				1	1	0	6
				1	1	1	7
3..6	dcti_threshold		0000	DCTI threshold (0,1,2,...,14,15)			
7	dcti_ddx_sel		1	DCTI ddx_sel 0: low 1: high			

Table 46: I²C Translater Register 7 (DCTI_1): Subaddress 37 hex

Bit	Name	Host address (hex)	Default value (hex)	Function		
0..1	dcti limit	01D2	10	Bit1	Bit0	DCTI limit
				0	0	0
				0	1	1
				1	0	2
				1	1	3
2	dcti_separate		0	0: off 1: on		
3	dcti_protection		0	0: off 1: on		
4	dcti_filteron		1	0: off 1: on		
5	dcti_superhill		1	0: off 1: on		
6...7	nrln_0		00	DCTI number lines (2 LSBs)		

Table 47: I²C Translater Register 8 (DCTI_2): Subaddress 38 hex

Bit	Name	Host address (hex)	Default value (hex)	Function
0 ... 7	nrln_1	01D3	0FF	DCTI number lines upper 8 bits

Table 48: I²C Translater Register 9 (DCTI_3): Subaddress 39 hex

Bit	Name	Host address (hex)	Default value (hex)	Function
0 ... 7	nrpx	01D4	0D8	DCTI number of pixels / 4

Table 49: I²C Translater Register 10 (SIDEP_OVL_UV): Subaddress 3A hex

Bit	Name	Host address (hex)	Default value (hex)	Function
0 ... 3	overlay_u	01D5	1000	sidepanels overlay U 4 MSB
4 ... 7	overlay_v		1000	sidepanels overlay V 4 MSB

Table 50: I²C Translater Register 11 (SIDEP_OVL_Y): Subaddress 3B hex

Bit	Name	Host address (hex)	Default value (hex)	Function
0 ... 7	overlay_y	01D6	00	sidepanels overlay Y 8 MSB

Table 51: I²C Translater Register 12 (PEAKING): Subaddress 3C hex

Bit	Name	Host address (hex)	Default value (hex)	Function		
0..1	peak_a	01D7	01	Bit1	Bit0	peaking a
				0	0	0
				0	1	1/2
				1	0	1
				1	1	2
2..3	peak_b		01	Bit1	Bit0	peaking b
				0	0	0
				0	1	1/2
				1	0	1
				1	1	2
4..5	peak_limit		01	Bit1	Bit0	peak limiter setting
				0	0	255
				0	1	340
				1	0	425
				1	1	511
6..7	peak_coring		01	Bit1	Bit0	peak coring settings
				0	0	0
				0	1	4
				1	0	8
				1	1	16

Table 52: I²C Translater Register 13 (SIDEP_START) Subaddress 3D hex

Bit	Name	Host address (hex)	Default value (hex)	Function
0 ... 7	sidepanel_start	01D8	00	sidepanel start position (8 MSB)

Table 53: I²C Translater Register 14 (SIDEP_STOP): Subaddress 3E hex

Bit	Name	Host address (hex)	Default value (hex)	Function
0 ... 7	sidepanel_stop	01D9	00	sidepanels stop position (8 MSB)

Table 54: I²C Translater Register 15 (SIDEP_FDEL): Subaddress 3F hex

Bit	Name	Host address (hex)	Default value (hex)	Function		
0...1	sidepanel_fdel	01DAh	00	Bit1	Bit0	sidepanel fine delay
				0	0	0
				0	1	1
				1	0	2
				1	1	3
2	display_mode		0	display mode 0: 9 bit, blanking level 288 1: 10 bit, blanking level 64		
3	uv_inv		0	0: default 1: invert UV input		
4, 5, 6	ydelay_out		0	lsb Y delay out		
			0	bit 1, Y delay out		
			0	msb Y delay out		
7	ena_hdsp_rst		0	0: default 1: enable HDSP reset		

3.2.4 Acknowledgement of bytes

The IPQ µC acknowledges always all register bytes independent from their contents. If the master µC transmits more than the maximum number of register bytes, the slave µC will acknowledge the following bytes, but will not store them in its internal RAM.

3.3 Receiving data from the IPQ µC

The IPQ µC is able to transmit one status byte plus additional read bytes to the main µC. The IPQ µC then works as a slave transmitter.

The I²C-bus transmission protocol for transmitting the status byte plus read registers has the following format:

Start	Slave address 69h	Ack	Status byte	ReadReg1	Ack	...	Nack	Stop

3.3.1 Contents of status byte

The status byte contains the following information:

Table 55: I²C Read Register 1 (STATUS): No Subaddress !

Bit	Name	Default value (hex)	Function
0	NON_IL	0	0: non interlaced mode not active 1: non interlaced mode active
1	FEATURE_MODE	0	0: default, no feature mode detected 1: feature mode detected
2	AUTO_MOVIE_FLAG	0	0: normal mode 1: automatic movie mode activated
4	MOVIE_FLAG		0: no movie mode detected 1: movie detected
4	PHASE_FLAG	0	0: standard mode (ABAB in case of MOVIE=1) 1: 180° phase shift (BCBC, MOVIE=1)
5	SCREEN_FADE_ACTIVE	0	0: screen fade not active 1: screen fade active
6	READY	1	0: not ready to accept command 1: ready to accept command
7	WATCH	0	Watchdog bit: will be toggled when status byte is read by master µC, initialized with 0

Bit 6 will be cleared after the IPQ µC has received I²C register bytes. It will be set again after the evaluation of all bytes is completed and an external interrupt (V100) initiating data transfer from IPQ µC to BESIC, datapath additional registers, PROZONIC/MELZONIC is not currently serviced.

3.3.2 Contents of datapath read registers

Table 56: I²C Read Register 2 (SCREEN_FADE_COUNT): No Subaddress !

Bit	Name	Function
0...7	SCREEN_FADE_COUNT	00: video completely faded out 01...67 hex: fade positions 68: video completely faded in

Table 57: I²C Read Register 3 (MPD MSByte1): No Subaddress !

Bit	Name	Function
0...7	MOVIE_PHASE_A	direct PROZONIC/MELZONIC register read, MSByte; Movie phase detection byte 1

Table 58: I²C Read Register 4 (MPD MSByte2): No Subaddress !

Bit	Name	Function
0...7	MOVIE_PHASE_B	direct PROZONIC/MELZONIC register read, MSByte; Movie phase detection byte 2

Table 59: I²C Read Register 5 (read_Uclerror): No Subaddress! (not available for digital acquisition concept)

Bit	Name	Host address (hex)	Function
0...6	read_Uclerror	0170	Read U channel clamp error (+3/-4 resolution 1/16 LSB)
7			reserved

Table 60: I²C Read Register 6 (read_Vclerror): No Subaddress! (not available for digital acquisition concept)

Bit	Name	Host address (hex)	Function
0...6	read_Vclerror	0171	Read V channel clamp error (+3/-4 resolution 1/16 LSB)

**Table 60: I²C Read Register 6 (read_Vclerror): No Subaddress!
(not available for digital acquisition concept)**

Bit	Name	Host address (hex)	Function
7			reserved

**Table 61: I²C Read Register 7 (read_Ygain): No Subaddress !
(not available for digital acquisition concept)**

Bit	Name	Host address (hex)	Function
0...7	read_Ygain	0172	Read overflow indication of Y channel

**Table 62: I²C Read Register 8 (AGC_Y_read): No Subaddress !
(not available for digital acquisition concept)**

Bit	Name	Host address (hex)	Function
0...7	AGC_Y_read	0173	AGC gain for Y channel, upper 8 bits (for functional test only)

3.4 Timing aspects

The maximum allowed response time between accepting register bytes and the execution of the commands handled by the IPQ µC is 90 ms. This time is only relevant when field memory control modes are changed. Field memory control modes are f. ex. Movie, Natural Motion, LFR, Still, Multi-PIP mode. When a field memory control mode has been activated, the IPQ µC waits max. 40 ms until a new frame starts (4 x 100Hz field repetition time). Then it takes another 40 ms until one new frame has been completely transmitted in order to run the new mode.

The maximum allowed total clock stretch time within one I²C message caused by a VDFL higher priority interrupt handling of the IPQ µC is 5 ms.

The minimum wait time between sending two I²C bus register data packages varies from 12 ms (no field memory control modes have changed) to 90 ms (field memory control modes have changed).

If the user wants to make sure that a complete I²C bus register data package is transmitted without being interrupted by VDFL IRQ µC routine and the slave µC is free for I²C after the master µC transmits I²C data, the I²C data package should be transmitted between 3 and 5 ms after VDFL occured. The slave µC sets bit 6 of the status byte when it is ready to accept I²C commands.

Multi-PIP:

The time between one live PIP picture register command to another should not be shorter than 120 ms.

Screen fade:

As long as this mode is active (86 fields = 860 ms in normal mode), all other mode changes are ignored.

4. Evaluation of I²C-bus register data

4.1 Field memory control modes

4.1.1 Priorities

The different Field Control Modes of the IPQ module have different priorities. The following table shows which mode has the highest and which mode has the lowest priority. The priority structure must be taken into account when activating field control modes.

Table 63 Mode Priorities

Mode	Priority
INIT	highest
VZOOM	.
MPIP	.
SCREEN FADE	.
GENERATOR mode	.
FEATURE mode	.
NON_IL mode	.
Natural Motion (MELZONIC concept)	.
LFR mode (MELZONIC/PROZONIC concept)	.
AABB mode	lowest

4.1.2 Functional description

AABB mode [LFR=0]

This mode is the field memory control mode setting for LFR = 0. Other field memory control modes need to be deactivated also.

The AABB mode is a simple field repetition mode. The incoming fields are written into a field memory and read twice. The doubled fields are displayed on the same position on the screen. This results in an elimination of the large area flicker whereas the lineflicker remains visible because the interlace frequency has not been changed. The SAA 4974 supplies an adapted vertical synchronization pulse for a correct display of the output fields in this mode. A DC-coupled vertical deflection is recommended because the sequence of field lengths is 313, 312.5, 312, 312.5 for PAL. The AABB mode is the standard conversion mode for the single field memory concept. The mode is activated via the I²C control if no other conversion mode is activated (Control Bits: LFR, NATURAL_MOTION, SAT_MODE, VZOOM, MOVIE, VZOOM and STILL cleared).

Control mode: AABB (AABB display raster)

LFR mode [LFR] (MELZONIC/PROZONIC concept)

In the line-flicker reduction mode the output fields are built of the sequence of an original field A, a median filtered field A*, a second median filtered field B* and an original field B processed by the SAA 4991/SAA 4990. The median filter avoids the scrambling of motion phases for a video source with motion content. The interlacing frequency of 25 Hz from the source is doubled to 50 Hz. This results in an elimination of the line-flicker. The LFR mode can be combined with the vertical zoom function (I²C-Register subaddress 02).

Control mode: A A* B* B (ABAB display raster)

Natural Motion mode [NATURAL_MOTION] (MELZONIC concept)

The natural motion field rate up-conversion eliminates motion artefacts caused by simple 100 Hz conversion methods like AABB resulting in areas of unsharpness at moving edges. The natural motion algorithm has to be adapted to the motion resolution of the source. For a video source the motion resolution of the display is up-converted from 50 Hz to 100 Hz by the motion compensation. This means every display field has the correct motion phase versus time resulting in a continuous motion, which is free of artefacts. For a movie source with 25 Hz motion resolution the original frame is displayed first followed by a motion compensated second frame. This results in an up-conversion of the motion resolution from 25 Hz to 50 Hz for movie sources.

There are thresholds for the motion compensation which can be set via the I²C interface if the control bit ENA_NM_CONTROL is set otherwise default values are used. For the quality of the recursive block-matching algorithm in the SAA 4991 a threshold called RELIABILITY_SEL (I²C register subaddress 2A Hex) can be defined. This value is the limit for the estimation error for every block calculated as the sum of absolute differences. If the limit for the estimation error is exceeded the block is marked as “bad”. The calculated vector for this block will not be used. Additionally the SAA 4991 supplies a read register “number_of_bad_ranges”. If this value exceeds the threshold BAD_LIMIT the natural motion is switched off globally and a fall-back conversion mode (e.g. LFR) is activated. The threshold BAD_LIMIT can also be changed via I²C bus (I²C register subaddress 29 Hex).

Control Mode: A AB BC* BC (ABAB display raster)

Movie mode [MOVIE], Auto Movie mode [AUTO_MOVIE], Phase bit [PHASE]

A forced Movie processing of the motion compensation is activated if the MOVIE bit is set, NATURAL_MOTION=1 and AUTO_MOVIE=0. The bit PHASE (I²C register subaddress 1, Bit 5) allows to define the correct phase relation between the movie frame and the video signal. The bit defines whether the fields A and B or fields B and C contain the same motion phase.

The Auto movie mode is normally activated (AUTO_MOVIE=1) together with NATURAL_MOTION=1 (MELZONIC concept). The software can automatically detect the kind of input source to apply the correct processing. The detection is based on the read values of the Melzonic registers “vector_sum”. This sum of vector absolutes represents the amount of motion found between two incoming fields. The software investigates the vector sums of a whole frame to detect whether a video or a movie source is connected. If the two values show a large difference the converter can be switched to a vector based movie processing increasing the movement resolution from 25 Hz to 50 Hz. The annoying motion judder of movies is eliminated. The phase relation between the movie pictures and the video fields is taken into account. In case of a video source or scenes with no or small motion the video processing is active, increasing the movement resolution from 50 Hz to 100 Hz. This removes the unsharpness of moving edges compared to a simple field repetition 100 Hz converter.

If the AUTO_MOVIE bit is cleared, the converter is performing a motion compensation processing for video sources as long as the bit MOVIE is cleared . If MOVIE is set a movie motion compensation is activated. The phase relation to the incoming movie can be adapted via the control bit PHASE. The user is able to adapt the natural motion processing to the source via the bits MOVIE and PHASE by himself if the automatic movie detection routine has been switched off.

If the control bits AUTO_MOVIE and MOVIE are cleared while NATURAL_MOTION is set the converter runs in the video mode.

Generator Mode (G_MODE)

The bit G_MODE activates a stable 100 Hz display with a fixed field length of 312.5 lines. The display field length is not adapted according to the video source. If additionally the 27 MHz PLL is unlocked via the control bit PLLMID the display is also in a horizontally free running mode. The conversion mode is reduced to a four times

single field repetition (AAAA) in this unsychronized mode. This special mode can be used to get a stable OSD picture without a source or with a very noisy source. It does also improve the picture stability for a tuner channel search.

Sat-Mode [SAT_MODE] (MELZONIC/PROZONIC concept)

In the satellite mode all the four 100 Hz display fields are derived from the output of the median filter. The median filter eliminates details occurring in only one line. This fact can be used to suppress typical FM noise drop-outs which normally occur uncorrelated in the field. A bad satellite signal reception can be improved quite effectively in this mode without deteriorating the picture quality.

Progressive Scan Mode [PSC] (MELZONIC/PROZONIC concept)

If the bit PSC is set a progressive scan mode is activated. The deinterlacing function (line interpolation) is performed with the help of the MELZONIC median filter. This mode could be preferably used for NTSC sources. The number of lines per field (525 lines / 60 Hz) is doubled and additionally the line flicker is removed. For NTSC sources a reduction of the visibility of the line structure is more important than the reduction of large area flicker (60/120 Hz) because a 60 Hz display shows much less large area flicker than a 50 Hz display.

Forced Single Field Mode [FSFM]

If the control bit FSFM is set the converter processes a forced single field mode (AAAA).

Still picture [STP]

It is possible to activate a still picture function in every control mode of the 100 Hz converter. The processing of this option is adapted to the conversion mode being activated before.

For the conversion modes Natural Motion, LFR and PSC a frame based still picture is generated (AA*AA*) by the help of the median filter in the SAA 4991/SAA 4990. In all the other modes a single field still picture is processed (e.g. AABB, generator mode).
If Still picture is performed while Noise reduction is active, a noise reduced frozen picture will be displayed.

VZOOM mode [REG3] (MELZONIC/PROZONIC concept)

The vertical zoom feature is activated via the control bit VZOOM. The bits VZOOM_0 to VZOOM_3 define the zoom factor. The vertical zoom function can be combined with the conversion modes FSFM, LFR and Natural Motion. The zoom function is based on a frame processing (LFR and Natural Motion) to achieve a high performance line interpolation.

For LFR and FSFM the zoomfactors 1.06, 1.1, 1.15, 1.2, 1.25, 1.3, 1.33 and 1.5 and
for Natural Motion the zoomfactors 1.1, 1.25, 1.33 and 1.5 are supported.

In the LFR and FSFM mode the software automatically centers the zoomed picture on the screen in vertical direction. This can be used for a smooth changing of the zoom factor by activating intermediate steps. If the FSFM bit is set a change from a high zoom factor to a low one can be performed without any temporary vertical displacements of the display.

Multi PIP function [Subaddress: 3] (MELZONIC/PROZONIC concept)

The 3x3 Multi-PIP feature uses the field memories of the 100 Hz converter to support a Multi-PIP display in combination with an external PIP module. This function can be used for a channel overview or photo-finish. A Photo-finish shows a sequence of frozen pictures of one source stored with constant time steps. The PIP display is assumed to be positioned at the bottom right of the screen. The PIP information is written to the desired MPIP position in the memory defined by the control bits POS0 to POS3. If a NTSC source shall be displayed in the MPIP portrayal the control bit SPIP (I²C register subaddress 3) has to be set.

4.2 Secondary control commands

4.2.1 General

Secondary control commands are:
(*: all combinable)

- Acquisition field frequency (*)
- Initialization command
- Adaptive noise reduction (Melzonic/Prozonic concept)
- Split screen (Melzonic/Prozonic concept)
- Screen fade
- Peaking (*)
- CTI (*)
- Port settings (*)
- HWE delay setup control (*)
- VWE delay setup control (*)

4.2.2 Acquisition field frequency [AFF]

The acquisition field frequency can be switched to 60 Hz (NTSC) by setting the AFF bit in REG1.

4.2.3 Initialization command [INIT]

If the INIT bit is set, default values are transmitted to the ICs in the concept. For the single field memory concept only the SAA 4974 is initialized. In the Melzonic/Prozonic concept additionally the SNERT registers of the SAA 4991/SAA 4990 are written.

The I²C registers of the SAA 4974 are initialized as listed in the following table. Some registers which optionally allow a direct control of signals and values are not activated via the initialization. The register contents are listed as an information which default values are used by the software. There is no need to transmit those registers as long as the direct access is not activated.

TABLE 64 Init Settings

I²C-Register, subaddress (Hex)	default value (Hex), (na) = not activated
00	00
01	01
02	10
03	00
04	00
05	00
06	00
07	00
08	80
09	10
0A	30

TABLE 64 Init Settings

I²C-Register, subaddress (Hex)	default value (Hex), (na) = not activated
0B	28 (na)
0E	1F (na)
0F	C3 (na)
10	00 (na)
11	AA (na)
12	0A (na)
13	52 (na)
14	F2 (na)
15	32 (na)
16	02 (na)
17	06 (na)
18	05 (na)
19	A9 (na)
1C	15 (na)
1D	31 (na)
1E	00 (na)
1F	00 (na)
20	10 (na)
21	00 (na)
22	00 (na)
23	00 (na)
24	00 (na)
25	00 (na)
26	8F (na)
27	55 (na)
28	00 (na)
29	40 (na)
2A	30 (na)

4.2.4 Noise reduction [NR1][NR0] (MELZONIC/PROZONIC concept)

The noise reduction is based on recursive filtering. For the Melzonic approach the recursive filtering is done in the 100 Hz domain. The second field memory serves as the field delay and contains the noise reduced picture. The ratio between recirculated information and new data from the incoming source is adapted via a motion detector automatically. The motion detection bases on the investigation of luminance differences (absolute differences) calculated between the output of memory 1 (new data) and the old data from memory 2.

3 different motion-adaptive noise reduction curves are selectable via the I²C bus. These settings are also relevant for the amount of noise reduction when activating split screen.

If the bit SET_NR (I²C-register subaddress 9, bit 2) is set, the MELZONIC control registers for the noise reduction can directly be defined by the user via the I²C-register subaddress 22 to 28 hex.

In the single field memory concept with the SAA 4956 the recursive loop exists in the 50 Hz domain. The SAA 4956 has two read ports, one is used for the 100 Hz conversion the other one reads at 50 Hz the information of the stored field to be processed with the incoming data. The noise reduction is directly controlled via the I²C bus interface of the SAA 4956.

4.2.5 Split screen [SPS1][SPS0] (MELZONIC/PROZONIC concept)

The split screen command declares a box in which the currently active adaptive noise reduction is enabled whereas the rest of the screen is displayed with noise reduction switched off. The box may split the screen display in two halves horizontally or vertically. Split screen will not be activated if noise reduction is switched off.

4.2.6 Screen fade [SCF0][SCF1]

The screen fade feature can be used to “fade out” a picture like closing curtains. This is done by the control SW by continuously changing the setting of the horizontal blanking for the DAC until a completely black picture is visible. The function is also available the other way round where the picture is “faded in” starting from a black display.

4.2.7 Set µC port bits [P11][P12][P14][P15]

Function:

This function enables the µC master to set/clear IPQ port bits via the I²C bus. The user is able to generate signals for own purposes on the IPQ board.

4.2.8 Fill option [FILL]

The fill option directly displays a defined background color on the screen. The color is selected via I²C subaddresses 20 hex and 21 hex (FIXCOL_Y, FIXCOL_UV).

4.2.9 HWE delay setup function [HWEFx]

By changing the bits HWEF0..HWEF3 (I²C subaddress 8) the default values of HWESTA/STO and HAMSBDEL (HWE1 fine delay) are modified.

The default value for HWESTA/STO can be decremented by max. 8 steps (HWEF0...HWEF3 = 0) or incremented by max. 7 steps (HWEF0...HWEF3 = 1). Each step for the correction equals 2 acquisition clocks, so that the chroma sequence is not disturbed. If the default setting shall not be changed, the setting HWEF0..HWEF2 = 0, HWEF3 = 1) has to be transmitted by the master µC via the I²C bus.

In case SET_HWE_MAIN_DELAY=1 (Subaddress 5, MSB), a coarse shift of HWE is possible via I²C subaddress 15 hex. The given values are directly added to the HWESTA/STO settings of the internal memory controller.

4.2.10 VWE delay function [VWEDx] [VWEX]

If the bit VWEX is set to 1, the vertical write window may be shifted by the bits VWED0...D6 with line accuracy. In case VWEX = 0, the normal mode (default vertical write window) is processed. The write window should be shifted between VWED6..D0 = 0 and 3Fh).

If the bits LFR or FSFM are set and the bit NATURAL_MOTION is cleared an automatical VWE delay control is done (see VZOOM). The VWE shift via the VWE delay register is only possible if the control bit MANU_SHIFT (I²C-Register subaddress 6, bit 2) is set additionally in these modes.

4.2.11 Peaking

The Peaking function is activated via the datapath control registers defined in [DPCR].

Datapath address: 01D7 hex

4.2.12 CTI

The CTI function is activated via the datapath control registers defined in [DPCR].

Datapath addresses: 01D1 hex (DCTI_0), 01D2 hex (DCTI_1), 01D3 hex (DCTI_2), 01D4 hex (DCTI_3).

5. INDEX